What is claimed is:

1. An integrated circuit comprising:

a. an analog to digital converter;

b. an FIR filter; and

c. an output mechanism selectively providing either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

2. The integrated circuit of claim 1 in which the output mechanism comprises an external pin on the integrated circuit to which a user can apply a control signal to control the selection of fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

3. The integrated circuit of claim 1 in which the output mechanism comprises an one or more bits on a register of the integrated circuit to which a user can set to control the selection of fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

4. The integrated circuit of claim 3 in which said one or more bits on a register of the integrated circuit are set over a serial port interface.

5. The integrated circuit of claim 1 in which the analog to digital converter is a delta sigma modulator.

6. The integrated circuit of claim 1 in which the FIR filter is a decimation filter.

7. A method of designing an integrated circuit having an FIR filter, comprising the step of providing an mechanism to permit a user to select either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

8. A method of fabricating an integrated circuit having an FIR filter, comprising the step of providing an mechanism to permit a user to select either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.